Code No: 58014 **Set No. 1**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
IV B.Tech. II Sem., II Mid-Term Examinations, April-2014
COMPUTER SYSTEM ORGANIZATION
Objective Exam

Name: _____ Hall Ticket No. | | | | | | A | | | | |

Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 10.

I. Choose the correct alternative:

1. DRAMs are _____ [ ]
   a) slower, cheaper, larger b)Faster, cheaper, smaller
   c) faster, cheaper, larger d)Faster, expensive, smaller

2. EEPROM: can be defined as_____ [ ]
   a)electrically erasable programmable ROM b)electronic extendable programming ROM
   c) electrically expandable problematic ROM d)electrically expandable programmable ROM

3. Cache Memory is _____ [ ]
   a) large in size, less speed b) small in size, high speed
   c) small size, low speed d)large in size, high speed

4. The processor doesn't need to wait for the memory write to be completed is called [ ]
   a)read buffer b) cache c) main memory d) Write buffer

5. The contents of TLB must be coherent with the contents of _____in the memory. [ ]
   a) page tables b) index tables c) hash table d) cache

6. Access time – seek time / rotational delay is also called_____ [ ]
   a)absolute time b) latency time c) turnaround time d) burst time.

7. To coordinate the transmission of data between sender and Receiver an asynchronous bus uses a _____protocol. [ ]
   a) Handshaking b) TCP c) IP d) HTTP

8. I/O devices and the memory share the same address space, the arrangement is called [ ]
   a)main memory b)Memory-mapped I/O c) temporary memory d) cache memory

9. Maximum speed of the system is limited by the _____ [ ]
   a)length of source code b)no. of CPU s c) Memory Bandwidth d)none of the above

10. Execution of Concurrent Events in the computing process to achieve faster Computational Speed is called _____ [ ]
    a) serial processing b) piping c)paging d) Parallel Processing

Cont.....2

II Fill in the Blanks:

11. The formula to find the Hit Rate and Miss Penalty is _____
12. The processor is able to access the cache while a miss is being serviced is called_____
13. The measure of memory bandwidth is_____
14. In Parallel Processing - VLIW refers to_____
15. Machine with a very fast clock cycle that executes at the rate of one instruction per cycle comes under_____
16. It becomes difficult to run many parallel wires at high speed due to _____
17. The number of special control lines required for hand-shaking is_____
18. In Memory mapped I/O the address of the input buffer associated with the Keyboard is _____
19. Parallel Computing, Distributed Computing, super, vector and Concurrent Computing are the Characteristics of _____
20. The Inter Processor Synchronization can be obtained with _____

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Code No: 58014 **Set No. 2**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
IV B.Tech. II Sem., II Mid-Term Examinations, April-2014
COMPUTER SYSTEM ORGANIZATION
Objective Exam

Name: _____ Hall Ticket No. | | | | | | A | | | | |

Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 10.

I. Choose the correct alternative:

1. The processor doesn't need to wait for the memory write to be completed is called [ ]
   a)read buffer b) cache c) main memory d) Write buffer

2. The contents of TLB must be coherent with the contents of _____in the memory. [ ]
   a) page tables b) index tables c) hash table d) cache

3. Access time – seek time / rotational delay is also called_____ [ ]
   a)absolute time b) latency time c) turnaround time d) burst time.

4. To coordinate the transmission of data between sender and Receiver an asynchronous bus uses a _____protocol. [ ]
   a) Handshaking b) TCP c) IP d) HTTP

5. I/O devices and the memory share the same address space, the arrangement is called [ ]
   a)main memory b)Memory-mapped I/O c) temporary memory d) cache memory

6. Maximum speed of the system is limited by the _____ [ ]
   a)length of source code b)no. of CPU s c) Memory Bandwidth d)none of the above

7. Execution of Concurrent Events in the computing process to achieve faster Computational Speed is called _____ [ ]
   a) serial processing b) piping c)paging d) Parallel Processing

8. DRAMs are _____ [ ]
   a) slower, cheaper, larger b)Faster, cheaper, smaller
   c) faster, cheaper, larger d)Faster, expensive, smaller

9. EEPROM: can be defined as_____ [ ]
   a)electrically erasable programmable ROM b)electronic extendable programming ROM
   c) electrically expandable problematic ROM d)electrically expandable programmable ROM

10. Cache Memory is _____ [ ]
    a) large in size, less speed b) small in size, high speed
    c) small size, low speed d)large in size, high speed

Cont.....2

II Fill in the Blanks:

11. In Parallel Processing - VLIW refers to_____

12. Machine with a very fast clock cycle that executes at the rate of one instruction per cycle comes under_____

13. It becomes difficult to run many parallel wires at high speed due to _____

14. The number of special control lines required for hand-shaking is_____

15. In Memory mapped I/O the address of the input buffer associated with the Keyboard is _____

16. Parallel Computing, Distributed Computing, super, vector and Concurrent Computing are the Characteristics of _____

17. The Inter Processor Synchronization can be obtained with _____

18. The formula to find the Hit Rate and Miss Penalty is _____

19. The processor is able to access the cache while a miss is being serviced is called_____

20. The measure of memory bandwidth is_____

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Code No: 58014 **Set No. 3**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
IV B.Tech. II Sem., II Mid-Term Examinations, April-2014
COMPUTER SYSTEM ORGANIZATION
Objective Exam

Name: _____ Hall Ticket No. | | | | | | A | | | | |

Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 10.

I. Choose the correct alternative:

1. Access time – seek time / rotational delay is also called_____ [ ]
a)absolute time b) latency time c) turnaround time d) burst time.

2. To coordinate the transmission of data between sender and Receiver an asynchronous bus uses a _____protocol. [ ]
a) Handshaking b) TCP c) IP d) HTTP

3. I/O devices and the memory share the same address space, the arrangement is called [ ]
a)main memory b)Memory-mapped I/O c) temporary memory d) cache memory

4. Maximum speed of the system is limited by the _____ [ ]
a)length of source code b)no. of CPU s c) Memory Bandwidth d)none of the above

5. Execution of Concurrent Events in the computing process to achieve faster Computational Speed is called _____ [ ]
a) serial processing b) piping c)paging d) Parallel Processing

6. DRAMs are _____ [ ]
a) slower, cheaper, larger b)Faster, cheaper, smaller
c) faster, cheaper, larger d)Faster, expensive, smaller

7. EEPROM: can be defined as_____ [ ]
a)electrically erasable programmable ROM b)electronic extendable programming ROM
c) electrically expandable problematic ROM d)electrically expandable programmable ROM

8. Cache Memory is _____ [ ]
a) large in size, less speed b) small in size, high speed
c) small size, low speed d)large in size, high speed

9. The processor doesn't need to wait for the memory write to be completed is called [ ]
a)read buffer b) cache c) main memory d) Write buffer

10. The contents of TLB must be coherent with the contents of _____in the memory. [ ]
a) page tables b) index tables c) hash table d) cache

Cont.....2

II Fill in the Blanks:

11. It becomes difficult to run many parallel wires at high speed due to _____
12. The number of special control lines required for hand-shaking is_____
13. In Memory mapped I/O the address of the input buffer associated with the Keyboard is _____
14. Parallel Computing, Distributed Computing, super, vector and Concurrent Computing are the Characteristics of _____
15. The Inter Processor Synchronization can be obtained with _____
16. The formula to find the Hit Rate and Miss Penalty is _____
17. The processor is able to access the cache while a miss is being serviced is called_____
18. The measure of memory bandwidth is_____
19. In Parallel Processing - VLIW refers to_____
20. Machine with a very fast clock cycle that executes at the rate of one instruction per cycle comes under_____

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Code No: 58014 **Set No. 4**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
IV B.Tech. II Sem., II Mid-Term Examinations, April-2014
COMPUTER SYSTEM ORGANIZATION
Objective Exam

Name: _____ Hall Ticket No. | | | | | | A | | | | |

Answer All Questions. All Questions Carry Equal Marks. Time: 20 Min. Marks: 10.

I. Choose the correct alternative:

1. I/O devices and the memory share the same address space, the arrangement is called [ ]
   a)main memory b)Memory-mapped I/O c) temporary memory d) cache memory

2. Maximum speed of the system is limited by the _____ [ ]
   a)length of source code b)no. of CPU s c) Memory Bandwidth d)none of the above

3. Execution of Concurrent Events in the computing process to achieve faster Computational Speed is called _____ [ ]
   a) serial processing b) piping c)paging d) Parallel Processing

4. DRAMs are _____ [ ]
   a) slower, cheaper, larger b)Faster, cheaper, smaller
   c) faster, cheaper, larger d)Faster, expensive, smaller

5. EEPROM: can be defined as_____ [ ]
   a)electrically erasable programmable ROM b)electronic extendable programming ROM
   c) electrically expandable problematic ROM d)electrically expandable programmable ROM

6. Cache Memory is _____ [ ]
   a) large in size, less speed b) small in size, high speed
   c) small size, low speed d)large in size, high speed

7. The processor doesn't need to wait for the memory write to be completed is called [ ]
   a)read buffer b) cache c) main memory d) Write buffer

8. The contents of TLB must be coherent with the contents of _____in the memory. [ ]
   a) page tables b) index tables c) hash table d) cache

9. Access time – seek time / rotational delay is also called_____ [ ]
   a)absolute time b) latency time c) turnaround time d) burst time.

10. To coordinate the transmission of data between sender and Receiver an asynchronous bus uses a _____protocol. [ ]
    a) Handshaking b) TCP c) IP d) HTTP

Cont.....2

II Fill in the Blanks:

11. In Memory mapped I/O the address of the input buffer associated with the Keyboard is _____

12. Parallel Computing, Distributed Computing, super, vector and Concurrent Computing are the Characteristics of _____

13. The Inter Processor Synchronization can be obtained with _____

14. The formula to find the Hit Rate and Miss Penalty is _____

15. The processor is able to access the cache while a miss is being serviced is called_____

16. The measure of memory bandwidth is_____

17. In Parallel Processing - VLIW refers to_____

18. Machine with a very fast clock cycle that executes at the rate of one instruction per cycle comes under_____

19. It becomes difficult to run many parallel wires at high speed due to _____

20. The number of special control lines required for hand-shaking is_____

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