Code No: 56059 **Set No. 1**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

III B.Tech. II Sem., II Mid-Term Examinations, April – 2014

ANALOG AND DIGITAL IC APPLICATIONS

Objective Exam

Name: _____ Hall Ticket No. | | | | | | A | | | | |

Answer All Questions. All Questions Carry Equal Marks.Time: 20 Min. Marks: 10.

I Choose the correct alternative:

1. The fastest A/D converter is_____ [ ]
   a) Successive approximation ADC b) Flash ADC c) counter type ADC d) servo tracking ADC

2. _____is the smallest change in voltage produced at the output of the D/A converter. [ ]
   a) Resolution b) Linearity c) Accuracy d) stability

3. The resolution of a 6-bit digital-to-analog converter (DAC) is: [ ]
   a) 63% b) 64% c) 1.588% d) 15.6%

4. The IC no. of 8-bit comparator is_____ [ ]
   a) 7485 b) 74138 c) 74150 d) 74682

5. A 24-bit group ripple adder can be designed using_____74283 ICs [ ]
   a) 2 b) 4 c) 6 d) 8

6. For divide-by -2 operation, the Flip-Flop must be in the _____ condition [ ]
   a) J=1, K=0 b) J=1, K=1 c) J=0, K=0 d) J=0, K=1

7. Terminal count of a modulus-13 binary counter is_____ [ ]
   a) 0000 b) 1111 c) 1101 d) 1100

8. To serially shift a byte of data into a shift register, there must be_____ [ ]
   a) one clock pulse b) one load pulse
   c) eight clock pulses d) one clock pulse for each 1 in the data

9. Which of the following is not a TTL circuit [ ]
   a) 74F00 b) 74AS00 c) 74HC00 d) 74ALS00

10. The noise margin of standard TTL logic is equal to [ ]
    a) 0.2 b) 0.4 c) 0.6 d) 0.8

Cont……2

II Fill in the blanks

11. _____ type ADCs compares a given analog signal with the internally generated equivalent signal.
12. _____ is used to find the required value of each bit by trial and error in successive approximation ADC.
13. The 74X138 3-to-8 decoder has _____enable inputs
14. The IC _____ is an 8-bit priority encoder.
15. A 32-to-1 multiplexer can be designed using_____ 8-to-1 multiplexers and _____ 2-to4-decoder.
16. A memory with 256 addresses has_____ address lines
17. The bit capacity of a memory that has 1024 addresses and can store 8 bits at each address is_____
18. CMOS operates more reliably than TTL in a high noise environment because of its_____
19. Open collector (or) open drain outputs can be connected together to form _____configuration.
20. The output circuit of a standard TTL inverter circuit consists of transistors in _____arrangement

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Code No: 56059 **Set No. 2**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

III B.Tech. II Sem., II Mid-Term Examinations, April – 2014

ANALOG AND DIGITAL IC APPLICATIONS

Objective Exam

Name: _____ Hall Ticket No. | | | | | | A | | | | |

Answer All Questions. All Questions Carry Equal Marks.Time: 20 Min. Marks: 10.

I Choose the correct alternative:

1. The IC no. of 8-bit comparator is_____ [ ]
   a) 7485 b) 74138 c) 74150 d) 74682

2. A 24-bit group ripple adder can be designed using_____74283 ICs [ ]
   a) 2 b) 4 c) 6 d) 8

3. For divide-by -2 operation, the Flip-Flop must be in the _____ condition [ ]
   a) J=1, K=0 b) J=1, K=1 c) J=0, K=0 d) J=0, K=1

4. Terminal count of a modulus-13 binary counter is_____ [ ]
   a) 0000 b) 1111 c) 1101 d) 1100

5. To serially shift a byte of data into a shift register, there must be_____ [ ]
   a) one clock pulse b) one load pulse
   c) eight clock pulses d) one clock pulse for each 1 in the data

6. Which of the following is not a TTL circuit [ ]
   a) 74F00 b) 74AS00 c) 74HC00 d) 74ALS00

7. The noise margin of standard TTL logic is equal to [ ]
   a) 0.2 b) 0.4 c) 0.6 d) 0.8

8. The fastest A/D converter is_____ [ ]
   a) Successive approximation ADC b) Flash ADC c) counter type ADC d) servo tracking ADC

9. _____is the smallest change in voltage produced at the output of the D/A converter. [ ]
   a) Resolution b) Linearity c) Accuracy d) stability

10. The resolution of a 6-bit digital-to-analog converter (DAC) is: [ ]
    a) 63% b) 64% c) 1.588% d) 15.6%

Cont……2

II Fill in the blanks

11. The IC _____ is an 8-bit priority encoder.

12. A 32-to-1 multiplexer can be designed using_____ 8-to-1 multiplexers and _____ 2-to4-decoder.

13. A memory with 256 addresses has_____ address lines

14. The bit capacity of a memory that has 1024 addresses and can store 8 bits at each address is_____

15. CMOS operates more reliably than TTL in a high noise environment because of its_____

16. Open collector (or) open drain outputs can be connected together to form _____configuration.

17. The output circuit of a standard TTL inverter circuit consists of transistors in _____arrangement

18. _____ type ADCs compares a given analog signal with the internally generated equivalent signal.

19. _____ is used to find the required value of each bit by trial and error in successive approximation ADC.

20. The 74X138 3-to-8 decoder has _____enable inputs

-oOo-

Code No: 56059 **Set No. 3**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

III B.Tech. II Sem., II Mid-Term Examinations, April – 2014

ANALOG AND DIGITAL IC APPLICATIONS

Objective Exam

Name: _____ Hall Ticket No. | | | | | | A | | | | |

Answer All Questions. All Questions Carry Equal Marks.Time: 20 Min. Marks: 10.

I Choose the correct alternative:

1. For divide-by -2 operation, the Flip-Flop must be in the _____ condition [ ]
   a) J=1, K=0 b) J=1, K=1 c) J=0, K=0 d) J=0, K=1

2. Terminal count of a modulus-13 binary counter is_____ [ ]
   a) 0000 b) 1111 c) 1101 d) 1100

3. To serially shift a byte of data into a shift register, there must be_____ [ ]
   a) one clock pulse b) one load pulse
   c) eight clock pulses d) one clock pulse for each 1 in the data

4. Which of the following is not a TTL circuit [ ]
   a) 74F00 b) 74AS00 c) 74HC00 d) 74ALS00

5. The noise margin of standard TTL logic is equal to [ ]
   a) 0.2 b) 0.4 c) 0.6 d) 0.8

6. The fastest A/D converter is_____ [ ]
   a) Successive approximation ADC b) Flash ADC c) counter type ADC d) servo tracking ADC

7. _____is the smallest change in voltage produced at the output of the D/A converter. [ ]
   a) Resolution b) Linearity c) Accuracy d) stability

8. The resolution of a 6-bit digital-to-analog converter (DAC) is: [ ]
   a) 63% b) 64% c) 1.588% d) 15.6%

9. The IC no. of 8-bit comparator is_____ [ ]
   a) 7485 b) 74138 c) 74150 d) 74682

10. A 24-bit group ripple adder can be designed using_____74283 ICs [ ]
    a) 2 b) 4 c) 6 d) 8

Cont……2

II Fill in the blanks

11. A memory with 256 addresses has_____ address lines

12. The bit capacity of a memory that has 1024 addresses and can store 8 bits at each address is_____

13. CMOS operates more reliably than TTL in a high noise environment because of its_____

14. Open collector (or) open drain outputs can be connected together to form _____configuration.

15. The output circuit of a standard TTL inverter circuit consists of transistors in _____arrangement

16. _____ type ADCs compares a given analog signal with the internally generated equivalent signal.

17. _____ is used to find the required value of each bit by trial and error in successive approximation ADC.

18. The 74X138 3-to-8 decoder has _____enable inputs

19. The IC _____ is an 8-bit priority encoder.

20. A 32-to-1 multiplexer can be designed using_____ 8-to-1 multiplexers and _____ 2-to4-decoder.

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Code No: 56059 **Set No. 4**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

III B.Tech. II Sem., II Mid-Term Examinations, April – 2014

ANALOG AND DIGITAL IC APPLICATIONS

Objective Exam

Name: _____ Hall Ticket No. | | | | | | A | | | | |

Answer All Questions. All Questions Carry Equal Marks.Time: 20 Min. Marks: 10.

I Choose the correct alternative:

1. To serially shift a byte of data into a shift register, there must be_____ [ ]
   a) one clock pulse b) one load pulse
   c) eight clock pulses d) one clock pulse for each 1 in the data

2. Which of the following is not a TTL circuit [ ]
   a) 74F00 b) 74AS00 c) 74HC00 d) 74ALS00

3. The noise margin of standard TTL logic is equal to [ ]
   a) 0.2 b) 0.4 c) 0.6 d) 0.8

4. The fastest A/D converter is_____ [ ]
   a) Successive approximation ADC b) Flash ADC c) counter type ADC d) servo tracking ADC

5. _____is the smallest change in voltage produced at the output of the D/A converter. [ ]
   a) Resolution b) Linearity c) Accuracy d) stability

6. The resolution of a 6-bit digital-to-analog converter (DAC) is: [ ]
   a) 63% b) 64% c) 1.588% d) 15.6%

7. The IC no. of 8-bit comparator is_____ [ ]
   a) 7485 b) 74138 c) 74150 d) 74682

8. A 24-bit group ripple adder can be designed using_____74283 ICs [ ]
   a) 2 b) 4 c) 6 d) 8

9. For divide-by -2 operation, the Flip-Flop must be in the _____ condition [ ]
   a) J=1, K=0 b) J=1, K=1 c) J=0, K=0 d) J=0, K=1

10. Terminal count of a modulus-13 binary counter is_____ [ ]
    a) 0000 b) 1111 c) 1101 d) 1100

Cont……2

II Fill in the blanks

11. CMOS operates more reliably than TTL in a high noise environment because of its_____

12. Open collector (or) open drain outputs can be connected together to form _____configuration.

13. The output circuit of a standard TTL inverter circuit consists of transistors in _____arrangement

14. _____ type ADCs compares a given analog signal with the internally generated equivalent signal.

15. _____ is used to find the required value of each bit by trial and error in successive approximation ADC.

16. The 74X138 3-to-8 decoder has _____enable inputs

17. The IC _____ is an 8-bit priority encoder.

18. A 32-to-1 multiplexer can be designed using_____ 8-to-1 multiplexers and _____ 2-to4-decoder.

19. A memory with 256 addresses has_____ address lines

20. The bit capacity of a memory that has 1024 addresses and can store 8 bits at each address is_____

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