Code No: 56029 **Set No. 1**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

III B.Tech. II Sem., II Mid-Term Examinations, April – 2014

VLSI DESIGN

Objective Exam

Name: _____ Hall Ticket No. | | | | | | A | | | | |

Answer All Questions. All Questions Carry Equal Marks.Time: 20 Min. Marks: 10.

I Choose the correct alternative:

1. Good observability and controllability reduces number of test vectors required for_____ [ ]
   A. CMOS Testing B. manufacturing test C. Chip level Test D. built in self test

2. The limitation of serial/parallel multiplier is that _____ frequency is limited by the propagation through the array of adders. [ ]
   A. maximum B. minimum C. same D. none

3. Which of the following is not related in implementation of a logic/binary cell for storing one-bit [ ]
   A. 2 inputs and 1 output
   B. data input
   C. select input enables the cell for reading and writing.
   D. read/write input determines the cell operation when it is selected.

4. Which of the following is a volatile type of memory [ ]
   A. DRAM B. SRAM C. Flash D. none

5. Which of the following are process technologies in CPLD [ ]
   A. EPROM, EEPROM and FLASH B. SRAM, ANTIFUSE & EEPROM
   C. FLASH, SRAM and ANTIFUSE D. FLASH, SRAM & ANTIFUSE

6. In commercial FPGS chips, Look Up Tables usually have either 4 or 5 inputs which require _____ storage cells. [ ]
   A. 16 and 24 B. 16 and 32 C. 8 and 16 D. 12 and 24

7. A comparator is build with an _____ and an _____ [ ]
   A. adder, or B. adder, inverter C. and, inverter D. adder, and

8. Which of the following allows a larger no. of array elements to be utilized than a channeled array for the same size of die [ ]
   A. sea of gate arrays B. channel gate array
   C. structured gate array D. none of the above

9. An embedded gate array or structured gate array is a combination of [ ]
   A. CBIC B. MGA C. both A and B D. none

10. Process of converting unoptimized Boolean description to a PLA format is known as [ ]
    A. translation B. flattening C. mapping D. factoring

Cont.....2

II Fill in the blanks

11. The _____ breaks the carry computation in to two steps starting with the computation of two intermediate values.

12. _____ is the process of optimizing Boolean equation at the logic level and mapping them to a techno-specific library of cells.

13. _____ is the process of splitting a single design among multiple devices.

14. JTAG stands for _____

15. _____ are used to control the output of the optimization and mapping process.

16. _____ is a degree to which it can be observed that node at output operates correctly.

17. _____ provides fixed interconnection of along with its four sides.

18 Fault coverage is defined as the percentage of fault that can be detected by the applied _____

19. A _____ is tested by shifting a special pattern through the scan path before stuck at faults begins.

20. _____ provides each wire a route through a set of areas and avoids wasting of chip area

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Code No: 56029 **Set No. 2**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

III B.Tech. II Sem., II Mid-Term Examinations, April – 2014

VLSI DESIGN

Objective Exam

Name: _____ Hall Ticket No. | | | | | | A | | | | |

Answer All Questions. All Questions Carry Equal Marks.Time: 20 Min. Marks: 10.

I Choose the correct alternative:

1. Which of the following is a volatile type of memory [ ]
   A. DRAM B. SRAM C. Flash D. none

2. Which of the following are process technologies in CPLD [ ]
   A. EPROM, EEPROM and FLASH B. SRAM, ANTIFUSE & EEPROM
   C. FLASH, SRAM and ANTIFUSE D. FLASH, SRAM & ANTIFUSE

3. In commercial FPGS chips, Look Up Tables usually have either 4 or 5 inputs which require _____ storage cells. [ ]
   A. 16 and 24 B. 16 and 32 C. 8 and 16 D. 12 and 24

4. A comparator is build with an _____ and an _____ [ ]
   A. adder, or B. adder, inverter C. and, inverter D. adder, and

5. Which of the following allows a larger no. of array elements to be utilized than a channeled array for the same size of die [ ]
   A. sea of gate arrays B. channel gate array
   C. structured gate array D. none of the above

6. An embedded gate array or structured gate array is a combination of [ ]
   A. CBIC B. MGA C. both A and B D. none

7. Process of converting unoptimized Boolean description to a PLA format is known as [ ]
   A. translation B. flattening C. mapping D. factoring

8. Good observability and controllability reduces number of test vectors required for_____ [ ]
   A. CMOS Testing B. manufacturing test C. Chip level Test D. built in self test

9. The limitation of serial/parallel multiplier is that _____ frequency is limited by the propagation through the array of adders. [ ]
   A. maximum B. minimum C. same D. none

10. Which of the following is not related in implementation of a logic/binary cell for storing one-bit [ ]
    A. 2 inputs and 1 output
    B. data input
    C. select input enables the cell for reading and writing.
    D. read/write input determines the cell operation when it is selected.

Cont…….2

II Fill in the blanks

11. JTAG stands for _____

12. _____ are used to control the output of the optimization and mapping process.

13. _____ is a degree to which it can be observed that node at output operates correctly.

14. _____ provides fixed interconnection of along with its four sides.

15 Fault coverage is defined as the percentage of fault that can be detected by the applied _____

16. A _____ is tested by shifting a special pattern through the scan path before stuck at faults begins.

17. _____ provides each wire a route through a set of areas and avoids wasting of chip area

18. The _____ breaks the carry computation in to two steps starting with the computation of two intermediate values.

19. _____ is the process of optimizing Boolean equation at the logic level and mapping them to a techno-specific library of cells.

20. _____ is the process of splitting a single design among multiple devices.

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Code No: 56029 **Set No. 3**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

III B.Tech. II Sem., II Mid-Term Examinations, April – 2014

VLSI DESIGN

Objective Exam

Name: _____ Hall Ticket No. | | | | | | A | | | | |

Answer All Questions. All Questions Carry Equal Marks.Time: 20 Min. Marks: 10.

I Choose the correct alternative:

1. In commercial FPGS chips, Look Up Tables usually have either 4 or 5 inputs which require _____ storage cells. [ ]
   A. 16 and 24 B. 16 and 32 C. 8 and 16 D. 12 and 24

2. A comparator is build with an _____ and an _____ [ ]
   A. adder, or B. adder, inverter C. and, inverter D. adder, and

3. Which of the following allows a larger no. of array elements to be utilized than a channeled array for the same size of die [ ]
   A. sea of gate arrays B. channel gate array
   C. structured gate array D. none of the above

4. An embedded gate array or structured gate array is a combination of [ ]
   A. CBIC B. MGA C. both A and B D. none

5. Process of converting unoptimized Boolean description to a PLA format is known as [ ]
   A. translation B. flattening C. mapping D. factoring

6. Good observability and controllability reduces number of test vectors required for_____ [ ]
   A. CMOS Testing B. manufacturing test C. Chip level Test D. built in self test

7. The limitation of serial/parallel multiplier is that _____ frequency is limited by the propagation through the array of adders. [ ]
   A. maximum B. minimum C. same D. none

8. Which of the following is not related in implementation of a logic/binary cell for storing one-bit [ ]
   A. 2 inputs and 1 output
   B. data input
   C. select input enables the cell for reading and writing.
   D. read/write input determines the cell operation when it is selected.

9. Which of the following is a volatile type of memory [ ]
   A. DRAM B. SRAM C. Flash D. none

10. Which of the following are process technologies in CPLD [ ]
    A. EPROM, EEPROM and FLASH B. SRAM, ANTIFUSE & EEPROM
    C. FLASH, SRAM and ANTIFUSE D. FLASH, SRAM & ANTIFUSE

Cont.....2

II Fill in the blanks

11. _____ is a degree to which it can be observed that node at output operates correctly.

12. _____ provides fixed interconnection of along with its four sides.

13 Fault coverage is defined as the percentage of fault that can be detected by the applied _____

14. A _____ is tested by shifting a special pattern through the scan path before stuck at faults begins.

15. _____ provides each wire a route through a set of areas and avoids wasting of chip area

16. The _____ breaks the carry computation in to two steps starting with the computation of two intermediate values.

17. _____ is the process of optimizing Boolean equation at the logic level and mapping them to a techno-specific library of cells.

18. _____ is the process of splitting a single design among multiple devices.

19. JTAG stands for _____

20. _____ are used to control the output of the optimization and mapping process.

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Code No: 56029 **Set No. 4**

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

III B.Tech. II Sem., II Mid-Term Examinations, April – 2014

VLSI DESIGN

Objective Exam

Name: _____ Hall Ticket No. | | | | | | A | | | | |

Answer All Questions. All Questions Carry Equal Marks.Time: 20 Min. Marks: 10.

I Choose the correct alternative:

1. Which of the following allows a larger no. of array elements to be utilized than a channeled array for the same size of die [ ]
   A. sea of gate arrays B. channel gate array
   C. structured gate array D. none of the above

2. An embedded gate array or structured gate array is a combination of [ ]
   A. CBIC B. MGA C. both A and B D. none

3. Process of converting unoptimized Boolean description to a PLA format is known as [ ]
   A. translation B. flattening C. mapping D. factoring

4. Good observability and controllability reduces number of test vectors required for_____ [ ]
   A. CMOS Testing B. manufacturing test C. Chip level Test D. built in self test

5. The limitation of serial/parallel multiplier is that _____ frequency is limited by the propagation through the array of adders. [ ]
   A. maximum B. minimum C. same D. none

6. Which of the following is not related in implementation of a logic/binary cell for storing one-bit [ ]
   A. 2 inputs and 1 output
   B. data input
   C. select input enables the cell for reading and writing.
   D. read/write input determines the cell operation when it is selected.

7. Which of the following is a volatile type of memory [ ]
   A. DRAM B. SRAM C. Flash D. none

8. Which of the following are process technologies in CPLD [ ]
   A. EPROM, EEPROM and FLASH B. SRAM, ANTIFUSE & EEPROM
   C. FLASH, SRAM and ANTIFUSE D. FLASH, SRAM & ANTIFUSE

9. In commercial FPGS chips, Look Up Tables usually have either 4 or 5 inputs which require _____ storage cells. [ ]
   A. 16 and 24 B. 16 and 32 C. 8 and 16 D. 12 and 24

10. A comparator is build with an _____ and an _____ [ ]
    A. adder, or B. adder, inverter C. and, inverter D. adder, and

Cont.....2

II Fill in the blanks

11 Fault coverage is defined as the percentage of fault that can be detected by the applied _____

12. A _____ is tested by shifting a special pattern through the scan path before stuck at faults begins.

13. _____ provides each wire a route through a set of areas and avoids wasting of chip area

14. The _____ breaks the carry computation in to two steps starting with the computation of two intermediate values.

15. _____ is the process of optimizing Boolean equation at the logic level and mapping them to a techno-specific library of cells.

16. _____ is the process of splitting a single design among multiple devices.

17. JTAG stands for _____

18. _____ are used to control the output of the optimization and mapping process.

19. _____ is a degree to which it can be observed that node at output operates correctly.

20. _____ provides fixed interconnection of along with its four sides.

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